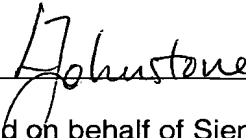## UNITED STATES PATENT AND TRADEMARK OFFICE

I, Lydia Johnstone, translator to Siemens Shared Services / Siemens Translation Services, of Hyde House, Oldbury, Bracknell, England declare:

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2.   That I am well acquainted with the German and English languages.

3.   That the attached is, to the best of my knowledge and belief, a true translation into the English language of the accompanying copy of the specification filed with the application for a patent in Germany on 31 July 2003 under the number PCT/DE03/02580 and the official certificate is attached hereto.

4.   That I believe that all statements made herein of my own knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application in the United States of America or any patent issuing thereon.

Johnstone

For and on behalf of Siemens Shared Services/
Siemens Translation Services

The _2_ day of _March_ , 2005

S4-02P11627

Description

5   Circuit arrangement for averaging

The invention relates to a circuit arrangement for averaging
according to the preamble of Claim 1.

10   In automotive engineering solenoid valves are known to be used
to control automatic transmission systems, being activated
with a pulse width modulated current signal. The average value
over time of the current is thereby determined, in order to be
able to optimize the control response of the solenoid valve
15   within a controlled system.

Conventional analog low-pass filters have hitherto been used
for this, which filter alternating current components out of
the current signal to a large extent and output the direct
20   current component as an average value.

Disadvantages of known averaging by means of analog filters
include the settling time of such filters, which means that
the average value is generally not available until after
25   several periods of pulse width modulation.

Averaging by means of analog filters is also relatively
inaccurate, which is equally undesirable.

30   The object of the invention is therefore to create a circuit
arrangement, which allows the fastest and most accurate
averaging possible.

The object is achieved by the characterizing features of Claim
1 based on a known circuit arrangement according to the
preamble of Claim 1.

The invention includes the general technical doctrine that a
summing unit or counter should be provided for averaging
between the signal input and the signal output of the circuit
arrangement.

Before the actual averaging process, the input signal to be
evaluated is thus preferably first digitized, so that
averaging can take place without the dynamic problems of
analog filters in the digital domain.

In a preferred embodiment of the invention the summing unit or
counter is connected on the input side to a sigma-delta
modulator, which subjects the input signal to be evaluated to
sigma-delta modulation and feeds the signal thus modulated to
the summing unit or counter. Such sigma-delta modulators are
for example known from NORSWORTHY/SCHREIER/TEMES: "Delta-Sigma
Data Converters" (IEEE Press), CANDY/TEMES: "Oversampling
Delta-Sigma Data Converters: Theory, Design and Simulation"
(IEEE Press) and ENGELEN/PLASSCHE: "Bandpass Sigma Delta
Modulators" (Kluwer Academic Publishers), the entire content
of which is to be considered part of the present description
in respect of the design of the sigma-delta modulator.

The sigma-delta modulator should thereby operate with a clock
frequency or sampling rate, which is greater than the Nyquist
rate of the input signal, so that oversampling takes place and
no signal information is lost from the input signal.

In the case of a periodic input signal, it is also
advantageous if the same time window of the input signal is
always evaluated. This is expediently the simple or multiple
5   period of the input signal. The counter therefore preferably
has a reset input, to which a control signal is fed, which is
generated for example by a micro-controller. The control
signal and the input signal to be evaluated preferably have a
temporally constant phase relationship to each other, so that
10   the same time window of the input signal is always evaluated.

In the case of a periodic input signal, it is also
advantageous, if the input signal and the clock signal of the
sigma-delta modulator have a temporally constant phase
15   relationship to each other, so that the same time window of
the input signal is always evaluated. The input signal for the
sigma-delta modulator is therefore preferably derived from the
clock signal to be evaluated, for which a conventional micro-
controller can be used for example.
20

It should also be pointed out that the sigma-delta modulator
can either be configured as analog or digital.

On the input side the sigma-delta modulator preferably has an
25   adding or subtracting unit and an integrator and on the output
side a comparator, the output of the comparator being fed back
in a feedback loop to an input of the adding or subtracting
unit.

30   The integrator of the sigma-delta modulator can for example be
configured as a first order integrator but higher order

integrators can also be used in the sigma-delta modulator,
resulting advantageously in a higher resolution.

5   The comparator arranged on the output side in the sigma-delta
    modulator has a predefined decision threshold, which
    preferably corresponds to a zero level of the input signal. If
    the value is above the decision threshold, the comparator
    preferably outputs a positive level, while if the value drops
    below the decision threshold, the comparator preferably
10 outputs a negative level.

    In a preferred embodiment of the invention the output of the
    comparator is not fed back directly to the input of the adding
    or subtracting unit in the feedback loop but to the controller
15 of a switching element, which switches either a first
    reference signal or a second reference signal to the input of
    the adding or subtracting unit. This is advantageous as the
    output signal of the comparator can contain inaccuracies,
    which are thus not fed back and therefore suppressed. The
20 reference signals can on the other hand be generated by
    reference signal sources with greater accuracy and
    consistency, so that the accuracy of the averaging process is
    enhanced by this indirect feedback.

25 In another variant of the invention however no sigma-delta
    modulator is required, an analog/digital converter being
    provided on the input side, which samples the analog input
    signal to be evaluated, converts it to a digital signal and
    then feeds it directly or indirectly to the summing unit or
30 counter. The average value over time of the input signal can
    then be determined easily from the number of previous
    samplings and the output signal of the summing unit or

counter, by dividing the output signal of the summing unit by
the number of accumulated sampling values.

The analog/digital converter should thereby also operate at a
5   sampling rate, which is greater than the Nyquist rate of the
input signal, so that oversampling takes place and no
signaling information is lost from the input signal.

In the case of a band-limited input signal with a predefined
10   upper limit frequency, the clock frequency of the
analog/digital converter is therefore preferably a whole
number multiple of the limit frequency of the input signal to
be evaluated, oversampling by a factor of 16, 32 or 64 being
advantageous, to achieve an adequate signal to noise ratio.
15

In the case of a periodic input signal, it is also
advantageous if the same time window of the input signal is
always sampled. The summing unit thereby preferably has a
reset input, to which a control signal is fed, which is
20   generated for example by a micro-processor. The control signal
and the input signal to be evaluated thereby have a temporally
constant phase relationship to each other, so that the same
time window of the input signal is always evaluated.

25   In the two variants described above with a sigma-delta
modulator in one case and a high-speed analog/digital
converter in the other, an output register is preferably
provided on the output side to buffer the average value, until
the next average value has been calculated.
30

The circuit arrangement according to the invention is
preferably suitable for averaging in the case of current and

voltage signals in automotive engineering. For example - as already indicated - the input signal to be evaluated can be a current signal, which is used to activate a solenoid valve.

5   It should also be pointed out that the circuit arrangement according to the invention does not necessarily have to be configured as a separate circuit. It is also possible for the circuit arrangement according to the invention to be part of a complex electronic circuit, which fulfils other functions in
10 addition to averaging.

Other advantageous developments of the invention are contained in the subclaims or are described below in conjunction with the description of the preferred exemplary embodiments of the
15 invention, with reference to the drawings, in which:

Figure 1   shows a circuit diagram of a circuit arrangement according to the invention with a sigma-delta modulator for averaging and
20 Figure 2   shows a circuit diagram of an alternative circuit arrangement with a high-speed analog/digital converter instead of a sigma-delta modulator.

The circuit arrangement shown in Figure 1 can for example be
25 used in an electronic transmission control system of a motor vehicle, to determine the average value over time of a current signal s.

To this end the circuit arrangement according to the invention
30 has a signal input 1, at which the current signal s to be evaluated is present.

Connected downstream from the signal input 1 is a sigma-delta modulator 2, which is analog in structure and comprises an adding unit 3, an integrator 4 and a comparator 5.

5   The adding unit 3 has a non-inverting input, which is connected to the signal input 1 of the circuit arrangement according to the invention and receives the input signal s.

The adding unit 3 also has an inverting input, which can
10 optionally be connected via a switching element 6 to one of two reference signal sources 7, 8. The reference signal source 7 hereby generates a reference signal Neg_Ref with a negative polarity, while the reference signal source 8 generates a reference signal Pos_Ref with a positive polarity.
15
Activation of the switching element 6 takes place as a function of the signal that appears at the output of the comparator 5. To this end the switching element 6 has a control input, which is connected to the output of the
20 comparator 5.

If the output signal of the comparator 5 has a positive polarity, the switching element 6 connects the inverting input of the adding unit 3 to the reference signal source 8.
25
If the output signal of the comparator 5 has a negative polarity however, the switching element 6 connects the inverting input of the adding unit 3 to the reference signal source 7.
30
This indirect feeding back of the comparator output to the inverting input of the adding unit has the advantage compared

with direct feeding back that the reference signal sources 7,
8 can generate a significantly more accurate and temporally
constant signal, while the output signal of the comparator 5
contains inaccuracies 5.

5

On the output side the adding unit 3 is connected to the input
of the integrator 4, the integrator 4 being a first order
integrator, to allow simple configuration with regard to
circuit engineering.

10

The integrator 4 is in turn connected on the output side to
the comparator 5, which compares the output signal of the
integrator 4 with a decision threshold, which corresponds to a
zero level of the input signal s.

15

If the value is above the decision threshold, the comparator 5
outputs an output signal with a positive polarity, so that the
switch 6 connects the inverting input of the adding unit 3 to
the reference signal source 8.

20

If the value is below the decision threshold however, the
comparator 5 outputs an output signal with a negative
polarity, so that the switch 6 connects the inverting input of
the adding unit 3 to the reference signal source 7.

25

Activation of the switch 6 and a counter 10 by the comparator
hereby takes place in a clock-controlled manner by means of a
clock signal CLK, which is generated by a micro-controller and
is present at a clock input 9. The clock frequency f_{CLK} of the
30   clock signal CLK is hereby twice the limit frequency f_s of the
band-limited input signal s, n being a whole number greater

than or equal to 1. This is expedient so that oversampling
takes place and no signal information is lost.

5 On the output side the sigma-delta modulator 2 is connected to
an enabling input ENABLE of the counter 10. A high level at
the enabling input ENABLE thus allows a counting process, in
which the counter reading is incremented in the counter 10.

The counter 10 also has a clock input CLOCK, which is
10 connected to the clock input 9 and thus is also activated by
the clock signal CLK.

The counter also has a reset input RESET, which is supplied
with a control signal CTRL, the control signal CTRL being
15 present at a control input 11 and being generated by a micro-
controller. It should be pointed out here that the control
signal CTRL is generated by the micro-controller such that
there is always a constant phase relationship between the
input signal s and the control signal CTRL. This means that
20 the same time window of the periodic input signal s is
evaluated in each instance, as the counter 10 is reset by the
control signal CTRL.

The counter reading of the counter 10 thus indicates the
25 average value over time of the input signal s during the
current period of pulse width modulation.

On the output side the counter 10 is connected to an output
register 12, which buffers the counter reading during the next
30 period. At the end of the next period the new counter reading
is transferred to the output register. The transfer of the
counter reading to the output register 12 is hereby controlled

by a control input LATCH, at which the control signal CTRL is
present.

The circuit arrangement according to the invention finally
5 outputs an output signal g at a signal output 13, indicating
the average value over time of the input signal s during the
last period.

The circuit diagram shown in Figure 2 showed a further
10 exemplary embodiment of a circuit arrangement according to the
invention for averaging, in which there is no need for a
sigma-delta modulator.

To receive an input signal s to be evaluated, this circuit
15 arrangement has a signal input 14, the input signal s possibly
being a current signal of an electronic transmission control
system in an automobile for example.

The input signal s is fed to a sampling input ANALOG IN of an
20 analog/digital converter 15, which generates a digital signal
Q_1 ... Q_n with a width of n bits from the input signal s.

The analog/digital converter 15 is hereby clocked by a clock
signal CLK, which is present at a clock input CLOCK of the
25 analog/digital converter 15 and determines the sampling rate.

The clock signal CLK is generated by a micro-controller, which
is not shown for the purposes of simplification, the clock
frequency of the clock signal CLK being essentially greater
30 than the limit frequency of the band-limited input signal s,
so that oversampling takes place and no signal information is
lost. In this exemplary embodiment the clock frequency of the

clock signal is 32 times the limit frequency of the input
signal s, giving a good signal to noise ratio.

On the output side the analog/digital converter 15 is
5   connected to a summing unit 16, which sums the digital signals
$Q_1 \ldots Q_n$ received on the input side and outputs a corresponding
digital signal $Q_1 \ldots Q_{n+m}$ with a word length of n+m bits on the
output side.

10   The summing unit 16 is hereby also clocked by the clock signal
CLK, so that all the digital signals $Q_1 \ldots Q_n$ sampled by the
analog/digital converter 15 are summed.

The summing unit 16 also has a reset input RESET, to which a
15   control signal CTRL is fed, which is generated by the micro-
controller (not shown). It should again be pointed out here
that the control signal CTRL is generated by the micro-
controller such that there is always a constant phase
relationship between the input signal s and the control signal
20   CTRL. This means that the same time window of the periodic
input signal s is evaluated in each instance, as the summing
unit 16 is reset by the control signal CTRL. Thus the sum $Q_1 \ldots$
Q_{n+m} of all the digital signals $Q_1 \ldots Q_n$ appears at the output of
the summing unit 16 during the current period in each
25   instance.

On the output side the summing unit 16 is connected to an
output register 17, which buffers the sum determined during
the next period. At the end of the next period the new summed
30   value is then transferred to the output register 17. The
transfer of the new summed value from the summing unit 16 to

the output register 17 is hereby controlled by a control input
LATCH, at which the control signal CTRL is present.

On the output side the output register 17 then outputs an
5   output signal $Q_1 \ldots Q_{n+m}$ at a signal output 18, said output
signal indicating the sum of the sampling values during the
last period. The average value over time during the last
period can then be calculated from this in conjunction with
the number of samplings or the sampling rate.
10

The invention is not restricted to the preferred exemplary
embodiments described above. Rather a plurality of variants
and modifications are possible, which also utilize the
inventive idea and therefore come into the scope of the
15   patent.